THAT WHICH IS CLAIMED IS:

1. A method for making a MOSFET comprising:

forming a trench in a semiconductor layer;

forming a gate dielectric layer lining the trench;

forming a gate conducting layer in a lower portion of the trench;

forming a dielectric layer to fill an upper portion of the trench;

removing portions of the semiconductor layer laterally adjacent the dielectric layer so that an upper portion thereof extends outwardly from the semiconductor layer;

forming spacers laterally adjacent the outwardly extending upper portion of the dielectric layer; and

using the spacers as a self-aligned mask for defining source/body contact regions.

2. A method according to Claim 1, wherein using the spacers as a self-aligned mask comprises implanting dopants for defining the source/body contact regions.

3. A method according to Claim 1, wherein using the spacers as a self-aligned mask comprises etching the semiconductor layer not covered by the spacers.

4. A method according to Claim 3, wherein the etching is performed to a depth equal to or less than about 1 micron from a surface of the semiconductor layer.

5. A method according to Claim 1, further comprising forming source regions in the semiconductor layer adjacent the outwardly extending dielectric layer before forming the spacers.

6. A method according to Claim 5, further comprising forming a source electrode on the source regions and on the dielectric layer.

7. A method according to Claim 6, further comprising forming at least one conductive via between the source electrode and the source/body contact regions.

8. A method according to Claim 5, further comprising forming a source electrode on the source regions, on the dielectric layer and on the source/body contact regions.

9. A method according to Claim 1, further comprising removing the spacers.

10. A method according to Claim 1, wherein removing portions of the semiconductor layer is performed to a depth equal to or less than about 1 micron from a surface thereof.

11. A method according to Claim 1, wherein the gate conducting layer is recessed in the trench within a range of about 0.2 to 0.8 microns from an opening thereof.

12. A method according to Claim 1, further comprising forming a body in the semiconductor layer adjacent the trench.

13. A method for making a MOSFET comprising:

forming a trench in a semiconductor layer;

forming a gate dielectric layer lining the trench;

forming a gate conducting layer in a lower portion of the trench;

forming a dielectric layer to fill an upper portion of the trench;

removing portions of the semiconductor layer laterally adjacent the dielectric layer so that an upper portion thereof extends outwardly from the semiconductor layer;

forming spacers laterally adjacent the outwardly extending upper portion of the dielectric layer;

using the spacers as a self-aligned mask for etching the semiconductor layer not covered by the spacers; and

using the spacers as a self-aligned mask for implanting dopants for defining source/body contact regions.

14. A method according to Claim 13, wherein the etching is performed to a depth equal to or less than about 1 micron from a surface of the semiconductor layer.

15. A method according to Claim 13, further comprising forming source regions in the semiconductor layer adjacent the outwardly extending dielectric layer before forming the spacers.

16. A method according to Claim 15, further comprising forming a source electrode on the source regions and on the dielectric layer.

17. A method according to Claim 16, further comprising forming at least one conductive via between the source electrode and the source/body contact regions.

18. A method according to Claim 15, further comprising forming a source electrode on the source regions, on the dielectric layer and on the source/body contact regions.

19. A method according to Claim 13, further comprising removing the spacers.

20. A method according to Claim 13, wherein removing portions of the semiconductor layer is performed to a depth equal to or less than about 1 micron from a surface thereof.

21. A method according to Claim 13, wherein the gate conducting layer is recessed in the trench within a range of about 0.2 to 0.8 microns from an opening thereof.

22. A method according to Claim 13, further comprising forming a body region in the semiconductor layer adjacent the trench.

23. A MOSFET comprising:

a semiconductor layer having a trench therein;

a gate dielectric layer lining the trench;

a gate conducting layer in a lower portion of the trench;

a dielectric layer in an upper portion of the trench and extending outwardly from said semiconductor layer;

source regions adjacent the outwardly extending dielectric layer; and

source/body contact regions laterally spaced from said gate conducting layer.

24. A MOSFET according to Claim 23, further further comprising a source electrode on said source regions and on said dielectric layer.

25. A MOSFET according to Claim 24, further comprising at least one conductive via between said source electrode and said source/body contact regions.

26. A MOSFET according to Claim 23, wherein a portion of said source regions include a recess over said source/body contact regions.

27. A MOSFET according to Claim 23, wherein a portion of said source regions include an opening exposing said source/body contact regions; and further comprising a source electrode on said source regions, on said dielectric layer, and on said source/body contact regions.

28. A MOSFET according to Claim 23, wherein said outwardly extending dielectric layer extends from said source regions equal to or less than about 1 micron.

29. A MOSFET according to Claim 23, wherein the gate is recessed in the trench within a range of about 0.2 to 0.8 microns from an opening thereof.

30. A MOSFET according to Claim 23, wherein said source/body contact regions are recessed within said semiconductor layer adjacent said source regions.

31. A MOSFET according to Claim 30, wherein an upper surface of the recess is equal to or less than a depth of about 1 micron from a surface of the semiconductor layer.